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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,209	12/22/2000	Wei-Fan Chen	B-4068 618463-2	1081

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/747,209	Applicant(s) CHEN, WEI-FAN	
	Examiner Dana Farahani	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 12, 13, 22, 23, 28, 31, and 35 are objected to because of the following informalities: lines 3, 4, 3, 3, 3, 4, and 3 of those claims, respectively, the word "resistor" should be "transistor".

Appropriate correction is required.

2. Claims 20 and 26 are objected to because of the following informalities: on line 3 of those claims, the phrase "conductivity type" should be "doping region".

Appropriate correction is required.

3. Claims 21, 22, and 29 are objected to because of the following informalities: the phrases "claim 1" and "claim 18" on line 2 of those claims should be "claim 17" and "claim 28", respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22, 24-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. 5869873), previously cited, in view of Dobkin (U.S. 4,153,909), newly cited.

Regarding claims 1, 11, 17, and 34, Yu discloses, figure 5, An electrostatic discharge protection circuit 5 with high trigger current, coupled to a node 1 and a reference potential Vss for dissipating the electrostatic voltage formed at the node, the electrostatic discharge protection circuit comprising: a substrate P-SUB having a first conductivity type, coupled to the reference potential Vss; a well region 50 having a second conductivity type, formed on the substrate and coupled to the node 1; a first doping region 52 having the first conductivity type; and a second doping region 54 having the second conductivity type, disposed on the substrate and electrically coupled to the reference potential; wherein, the electrostatic discharge current of said node provides a voltage with sufficient magnitude to breakdown the conjunction interface between said well region and said substrate, also triggering a BIPOLAR JUNCTION TRANSISTOR(BJT) comprising said well region, said substrate and said second doping region, for dissipating said electrostatic discharge current; and wherein said first doping area, when the electrostatic discharge current is greater than a predetermined current, reduces the potential difference between said node and said reference potential. Yu does not disclose the first doping region is electrically floated. Dobkin discloses in figure 12, a gated transistor 22 with floating node 36 to produce a gated SCR device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to make the first doping region in Yu's invention as a floating node in order to make a gated SCR device.

Regarding claims 2 and 18, Yu discloses, figure 5, the electrostatic discharge protection circuit further comprises a third doping area 57 having the second conductivity type, disposed in the well region, electrically coupled to the node, for forming an ohmic connection at the well region.

Regarding claims 3 and 19, Yu discloses, figure 5, the electrostatic discharge protection circuit, further comprises a forth doping region 56 having the first conductivity type, disposed at the surface of the substrate near said well region, electrically coupled to the reference potential Vss, for forming an ohmic connection at the substrate.

Regarding claims 4, 14-16, 32-33, and 37, Yu discloses the electrostatic discharge protection circuit wherein the first conductivity is p-type, and the second conductivity is n-type.

Regarding claims 5, 20, and 26, Yu discloses, in the figure, The electrostatic discharge protection circuit, wherein the electrostatic discharge circuit further comprises a fifth conductivity type 53 having the second conductivity type, disposed at the conjunction of the well region and the substrate, for reducing the breakdown voltage at the conjunction of said well region and said substrate.

Regarding claims 6, 21, and 27, Yu discloses, in the figure, the electrostatic discharge protection circuit, wherein the electrostatic discharge protection circuit further comprises a field oxide layer 551, disposed at the surface of the substrate adjacent to the fifth doping region.

Regarding claims 7-9, 12, 22, 24, 28-30, and 35, Yu discloses, in the figure, The electrostatic discharge protection circuit, wherein the electrostatic discharge protection circuit further comprises a MOS transistor 55 having a first conductivity type disposed on the substrate and comprising a gate 554 and two source/drain regions 53 and 54, wherein one of source/drain regions is electrically coupled to the well region, while the other of the source/drain regions, together with the gate, is electrically coupled to the reference potential.

Regarding claims 10, 25, 31, and 36, Yu discloses, figure 5, The electrostatic discharge protection circuit, wherein the electrostatic discharge protection circuit further comprises: a MOS transistor 55 having the first conductivity type, formed on the substrate, comprising a gate 554, and two source/drain regions 53 and 54, wherein one source/drain region is electrically coupled to the well region, and the other source/drain region is electrically coupled to the reference potential; a resistor R, its two ends electrically coupled to the gate and the reference potential, respectively; and a capacitor C of figure 6, its two ends electrically coupled to the gate and the node, respectively.

Regarding claim 13, Yu discloses, figure 6, The electrostatic discharge protection circuit, wherein the electrostatic discharge protection circuit comprises: a MOS transistor having the first conductivity type, comprising a gate, and two source/drain regions, wherein, one source/drain regions is electrically coupled to node 1, and the other source/drain is electrically coupled to the reference potential Vss; a resistor R, its two ends electrically coupled to the gate and the reference potential, respectively; and a capacitor C, its two ends electrically coupled to the gate and the node, respectively.

Response to Arguments

6. Applicant's corrections to the objected claims are acknowledged.

7. Applicant's arguments with respect to claims 1 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

This action is made **NON-FINAL**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
May 23, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800